REMARKS

Claims 1, 2, 5, 7, 11, 13, 14, 17, 19, 23, 25, 31, 35, 55, 60, 61, 72 and 74 are pending in the application. Initially, Applicants would like to thank the Examiner for the indication that claims 13, 14, 17, 19, 23, 25, 31, 35 and 74 are allowable. The Examiner has objected to claims 11 and 68 as being dependent upon a rejected base claim, but indicated that the claims would be allowable if rewritten in independent form including all of the limitations of any intervening claims.

The Examiner has rejected claims 1, 55 and 72 under 35 U.S.C. § 102(e) as allegedly anticipated by U.S. Patent No. 6,383,916 issued to Lin ("Lin"). Applicants respectfully submit the rejection is overcome in view of the remarks made herein.

To maintain a claim rejection under 35 U.S.C. § 102, a prior art reference must disclose each and every element of the claim. Lin fails to do so.

Independent claim 1 recites a semiconductor unit having two device terminals for every one input/output signal. The semiconductor unit comprises a laminated substrate and a semiconductor chip. The substrate comprises at least two wiring layers, which include a signal wiring layer and a power-supply or ground wiring layer. The substrate has a main surface. The semiconductor chip has an input/output pad and is mounted on the main surface of the laminated substrate through the input/output pad. Significantly, the two device terminals are mounted on the laminated substrate and connected to both ends of a signal wire in the signal wiring layer, while the signal wire is connected to the input/output pad of the semiconductor chip through a via hole (a configuration wherein the two terminals are wired to each other and the wire is connected to the pad through a via hole, see Fig. 6 of the application).

Independent claim 60 recites a semiconductor unit having two device terminals for every one input/output signal. The semiconductor unit comprises a laminated substrate and a semiconductor chip. The substrate comprises at least two wiring layers, which include a signal wiring layer and a power-supply or ground wiring layer. The substrate has a main surface and a back surface. The

semiconductor chip has an input/output pad and is mounted on the main surface of the laminated substrate. The two device terminals are disposed on the main surface and the back surface of the laminated substrate opposite to each other. Significantly, the two device terminals are connected to each other through a via hole, while the via hole is connected to the input/output pad of the semiconductor chip through a wire (a configuration wherein the two terminals are connected through a via hole and the via hole is wired to the pad, see Figs.23A and 23B).

Independent claim 61 recites a semiconductor unit having two device terminals for every one input/output signal. The semiconductor unit comprises a laminated substrate and two semiconductor chips. The substrate comprises at least two wiring layers including a signal wiring layer and a power-supply or ground wiring layer. The substrate has a main surface and a back surface. The semiconductor chips each have an input/output pad and are mounted on the main surface and the back surface of the laminated substrate, respectively. The two device terminals are disposed on the main surface and the back surface of the laminated substrate opposite to each other. Significantly, the two device terminals are connected to each other through a via hole, while the via hole is connected to the input/output pads of the semiconductor chip through a wire (a configuration wherein the two terminals are connected through a via hole and the via hole is wired to the pads, see Figs.26B and 26C).

Independent claim 55 recites a semiconductor unit having at least two device terminals for every one input/output signal. The two device terminals are disposed in different sides of the semiconductor unit. Significantly, the two device terminals are wired to an input/output pad of a semiconductor chip that corresponds to the input/output signal (a configuration wherein the two terminals are both wired to the pad, see Figs.18A and 18B).

Independent claim 72 recites a semiconductor unit comprising a semiconductor chip having an input/output pad and a package having a main surface and a back surface. The package comprises at least two ball terminal adhesive areas for every single input/output signal on the main and back surfaces of the package. A ball terminal is adhered to only one ball terminal adhesive area on one

surface of the package. Significantly, the two ball terminal adhesive areas are connected to each other through a via hole or a wire, and the via hole or wire is connected to the input/output pad the semiconductor chip through a wire (a configuration wherein two ball terminal adhesive areas are connected through a via hole or a wire and the via hoe or wire is connected to the pad through a wire, see Fig. 27A and 27B).

Thus, all of the independent claims recite, *inter alia*, the two device terminals are mutually connected to each other through a signal wire or a via hole formed in the laminated substrate, and the signal wire or via hole is further connected to the input/output pad of the semiconductor chip through a via hole or a signal wire.

Turning to the prior art, Lin discloses a method for forming a top metallization system for high performance integrated circuits, and a semiconductor structure formed by the method. Specifically, the Lin semiconductor structure is used to "elevate or fan-out the fine-line interconnects and to remove these interconnects from the micro and sub-micro level to a metal interconnect level that has considerable larger dimensions and is therefore with smaller resistance and capacitance and is easier and more cost effective to manufacture" (see Col. 6, Lines 49-54).

In view of this goal, Lin discloses a semiconductor structure as shown in Fig.1 of Lin. The semiconductor structure comprises a plurality of contact points (6), such as bonding pads, formed in the top surface of layer (3) and are part of the layer (3) (see Col.3, Lines 50-52 of Lin). These contact points (6) are the above-mentioned fine-line interconnects at the micro or sub-micro levels. The semiconductor structure further comprises pads (10, 11 and 12) formed on a thick polyimide layer (5) (see Col.4, Lines 3-5), which pads are connected to the contact points (6) through via holes (7). These pads (10, 11 and 12) are the above-mentioned metal interconnects and can be of any design in width and thickness to accommodate specific circuit design requirements. Thus, by the connection of the micro or sub-micro level contact points (6) to the metal level pads (10, 11,and 12), the micro or

sub-micro contacts points are accessible by the metal level pads. Lin discloses that a contact point is connected to a corresponding wider metal pad in a semiconductor structure.

Based on the foregoing underlying concept, Lin discloses, in Figs. 3a, 3b, 4 and 5 thereof, some examples of the arrangements and layouts of the metal level pads formed on the top layer of the Lin semiconductor structure (see Col. 5, Line 56 - Col. 6 Line 20).

Based on the foregoing underlying concept, Lin further discloses, in Figs. 9-11 thereof, an application of the concept to BGA chips, especially on how to fan-out and relocate the balls the BGA chips (see Col. 7 Lines 65-67). As shown in Figs. 9-11, the BGA chip (100) has a plurality of balls (101-105), which are disposed on the lower side of the chip and are relatively close to each other. In light of the Lin semiconductor structure shown in Fig. 1, Lin fans-out the closely located balls (101-105) by connecting the balls to another group of balls (111-115 in Fig. 9; 121-125 in Fig. 10; and 138-442 in Fig. 11), which are relatively larger and distributed so that the balls are not as crowded as balls (101-105). Thus, "the BGA pads can be arranged in a different and arbitrary sequence that is required for further circuit design or packaging" (see Col. 8, Lines 14-16 of Lin). The embodiment of BGA chip discloses that a smaller ball is connected to a lager ball, which is a variation of configuration shown in Fig. 1, a contact point connected to a corresponding wider metal pad.

In contrast, the present invention, as recited by the independent claims, disclose that two device terminals for every one input/output signal are mutually connected to each other through a signal wire or a via hole, and the signal wire or via hole is further connected to an input/output pad of a semiconductor chip through a via hole or a signal wire. Lin does not disclose the above feature.

In the Office Action, the Examiner alleges that Lin teaches two device terminals for every one input/output signal (Fig. 10, 101-105 and 121-125), a semiconductor chip (Fig. 10, 100) having an input/output pad (Fig. 5, Col. 6 lines 21-23 and Figs. 6 and 7), the two device terminals being connected to a wire (Fig. 10, 131) and the wire being connected to the input/output pad of the chip

through a via hole (Fig. 1, 7) (see the Paragraph 4, Page 2 and Paragraph 1, Page 3 of the Office Action). Applicants respectfully disagree for the following reasons.

As stated above, Lin discloses a semiconductor structure wherein the contact point is connected to a wider metal pad and a BGA chip wherein the ball of the chip is connected to another larger ball. However, Lin does not disclose that the wire (131) connecting balls (101-105) to balls (121-125), described in the embodiment of the BGA chip shown in Fig. 10, is further connected to the pads, described in the embodiment of semiconductor structure shown in Figs. 1, 5, 6 and 7. Nowhere does Lin disclose that wire (131) is connected to metal pads (10-12) through via hole (7). The Examiner has combined elements from different embodiments of Lin, to arrive at the combination of features recited in the independent claims of the present invention. However, neither of the embodiments disclose each and every limitation of the independent claims and nowhere does Lin disclose the combination of the above elements selected from the embodiments.

Therefore, Lin fails to disclose each and every element of claim 1, 55 and 72. Accordingly, the rejection of claims 1, 55 and 72 under 35 U.S.C. § 102(e) based on Lin is overcome.

The Examiner has rejected claims 2 and 61 under 35 U.S.C. § 103(a) as being unpatentable over Lin in view of U.S. Patent No. 6,137,164 issued to Yew et al. ("Yew"). The rejection is respectfully traversed.

Independent claim 1, from which claim 2 depends, and independent claim 61 are discussed above. Lin is discussed above relative to the independent claims.

Yew discloses an assembly for stacking IC devices. Yew is relied on to allegedly teach a substrate having two semiconductor chips mounted on the main surface and back surface respectively. However, Yew fails to overcome the underlying deficiencies identified in Lin. Therefore, Lin and Yew, taken alone or in any proper combination, fail to disclose or suggest the combination of features, as recited in Claims 2 and 61. Accordingly, the rejection of claims 2 and 61 under 35 U.S.C. § 103(a) over Lin in view of Yew is overcome and withdrawal thereof is respectfully requested.

The Examiner has rejected claim 5 under 35 U.S.C. § 103(a) as unpatentable over Yew in view of U.S. Patent No. 6,630,628 issued to Devnan et al. ("Devnan"). The rejection is respectfully traversed.

Independent claim 1, from which claim 5 depends, is discussed above. Yew is discussed above.

As shown above, Yew fails to disclose or suggest that two device terminals for every one input/output signal are mutually connected to each other through a signal wire or a via hole, and the signal wire or via hole is further connected to an input/output pad of a semiconductor chip through a via hole or a signal wire.

Devnan discloses a high-performance laminate for integrated circuit interconnection. Likewise, Devnan fails to disclose the above features, thus cannot overcome the underlying deficiencies identified in Yew. Therefore, Yew and Devnan, taken alone or in any proper combination, fail to disclose or suggest the combination of features, as recited in claim 1, from which claim 5 depends. Accordingly, the rejection of claim 5 under 35 U.S.C. § 103(a) over Yew in view of Devnan is overcome and withdrawal thereof is respectfully requested

The Examiner has further rejected claims 7 and 60 under 35 U.S.C. § 103(a) as unpatentable over Lin in view of U.S. Patent No. 6,184,477 issued to Tanahashi ("Tanahashi"). The rejection is respectfully traversed.

Independent claim 1, from which claim 7 depends, and independent claim 60 are discussed above.

Lin is discussed above relative to the independent claims.

Tanahashi discloses a multi-layer circuit substrate having orthogonal grid ground and power planes. Tanahashi is relied on to allegedly teach or suggest a signal layer between a power layer and a ground layer, the signal layer forming a strip line. Tanahashi fails to overcome the underlying deficiencies identified in Lin. Therefore, Lin and Tanahashi, taken alone or in any proper combination,

fail to disclose or suggest the combination of features of claims 7 and 60. Accordingly, the rejection of claims 7 and 60 under 35 U.S.C. § 103(a) over Lin in view of Tanahashi is overcome and withdrawal thereof is respectfully requested.

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application are believed to be in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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